

Problem 7: Cell Placement and Routing

Source: SpringSoft Inc.

February 15, 2000

1 Introduction

In this problem, we are concerned with the placement and routing for *row-based functional cells*. A row-based functional cell is an array of transistors in which all drain and source terminals of transistors of a given type, either pMOS or nMOS, lie along a single row of diffusion. Figure 1 shows the correspondence between the circuit symbol of a transistor and its corresponding layout in a functional cell. A transistor is formed where a polysilicon region crosses over a diffusion region. The polysilicon column of Figure 1(b) defines the *gate* terminal of the transistor, the diffusion region on one side of the polysilicon gives the *source* terminal, and the other diffusion region is the *drain* terminal. Such transistor layouts are typically placed end-to-end in a horizontal line, with vertical polysilicon columns (see Figure 1(c)). As shown in Figure 1(c), the upper array for the pMOS transistors implements the pullup subcircuit, and the lower one for the nMOS implements the pulldown subcircuit.

The gate terminals of transistors sharing the same column are typically connected together by polysilicon. A *diffusion gap* is needed to isolate transistor terminals that are physically adjacent in the cell but are not connected in the transistor circuit. Figure 1(c) shows transistors *c* and *d* separated by a diffusion gap because they are not connected in the pulldown subcircuit (see its corresponding circuit shown in Figure 2(a)). *Diffusion abutment*, which merges two neighboring diffusion regions, can be used if the physically adjacent terminals of the transistors in the cell are connected together in the corresponding circuit. Figure 1(c) shows transistors *b* and *c* connected by diffusion abutment because they are connected in both the pullup and pulldown subcircuits. A diffusion gap requires the separation between neighboring vertical polysilicon columns to be twice as large as that needed by diffusion abutment. Therefore, to reduce cell width, it is desirable to connect physically adjacent transistors by diffusion abutment.

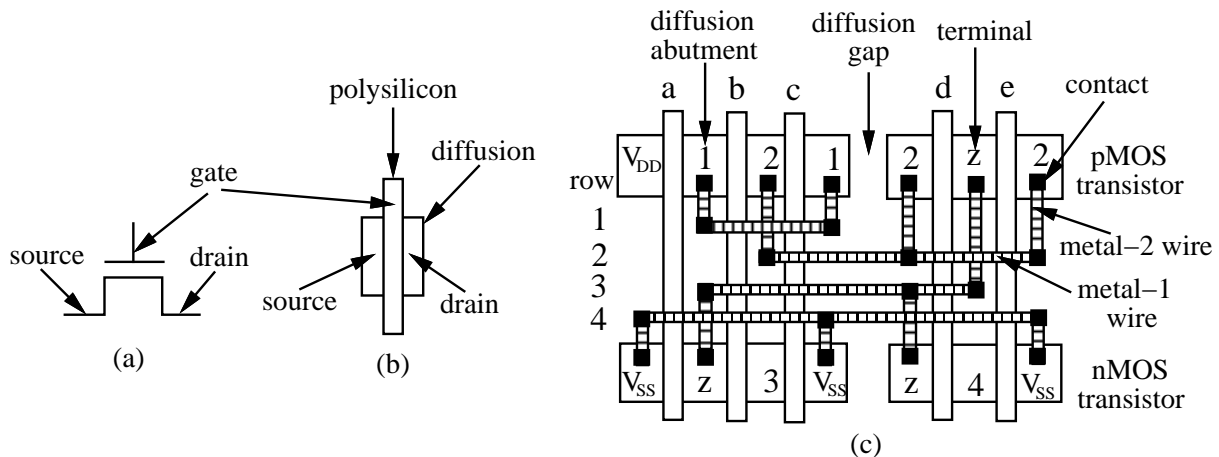


Figure 1: (a) Circuit symbol of an nMOS transistor; (b) layout of the transistor; (c) a row-based functional cell showing diffusion regions, metal wires, and transistor types.

The primary goal in functional cell design is to minimize the total area A in the final routing configura-

tion, which is approximated by the following formula:

$$A = H \times W, \quad (1)$$

where H and W are the height and width of the layout design, respectively. Here H is the number of rows in the layout, and W is computed by the summation of the number of actual columns (i.e., dual transistor pairs) and that of diffusion gaps. For example, the area of the layout shown in Figure 1(c) is given by $H \times W = 4 \times (5 + 1) = 24$ units. In the placement stage, however, the area A_p is typically estimated by

$$A_p = D \times W, \quad (2)$$

where D is the *density* in the cell design. By density, we mean the maximum number of wires in parallel anywhere in the cell design. For example, the density of the design shown in Figure 1(c) is four.

The polysilicon (gate) columns of a circuit can often be reordered without changing their logical function. The impact of reordering on layout area is illustrated by Figure 2, which shows a circuit implementing the function $z = \overline{a + bc + de}$. Figures 2(b), (c), and (d) give three alternatives of cell placement, with the respective densities of 4, 4, and 3 and the estimated areas of 24, 20, and 15 units. Note that the polysilicon columns d and e in Figure 2(c) are disconnected between the corresponding pMOS and nMOS transistors, and they thus contribute two units to the density. Figures 2(e), (f), (g) give corresponding cell routings, with the total areas of 24, 25, and 15 units, respectively.

2 Problem Description

The basic requirement of this problem is to develop a tool that finds a cell **placement** with the minimum area by reordering polysilicon columns. (Note that you are asked to do only *placement* to be eligible to enter this contest. Finishing a cell **routing**, however, is considered an advanced feature and is favorable to your contest grade. We will describe advanced features/functions in more detail in Section 5.)

The Cell Placement Problem is defined as follows.

- **Input:** Description of a transistor-level circuit.
- **Objective:** Develop a tool that finds a cell placement with the minimum area by reordering polysilicon columns.

3 Input

Input format is given as follows:

.SUBCKT	TEST		
Mx_1y_1	$drain_1$	y_1	$source_1$
Mx_2y_2	$drain_2$	y_2	$source_2$
...
$Mx_{2n}y_{2n}$	$drain_{2n}$	y_{2n}	$source_{2n}$
.END			

The first line of an input file starts with .SUBCKT, followed by the name of the circuit. The description of the transistor devices consists of $2n$ lines, with n lines for pMOS transistors and n lines for nMOS transistors (not necessarily in the order). Each line contains the name of the transistor Mx_iy_i , $1 \leq i \leq 2n$, with $x_i = P$ or N denoting the corresponding type of the transistor, followed by the three terminals, drain, gate (y_i), and source. The word .END in the input line signifies the end of input.

Here gives a sample input file for the circuit shown in Figure 2(a).

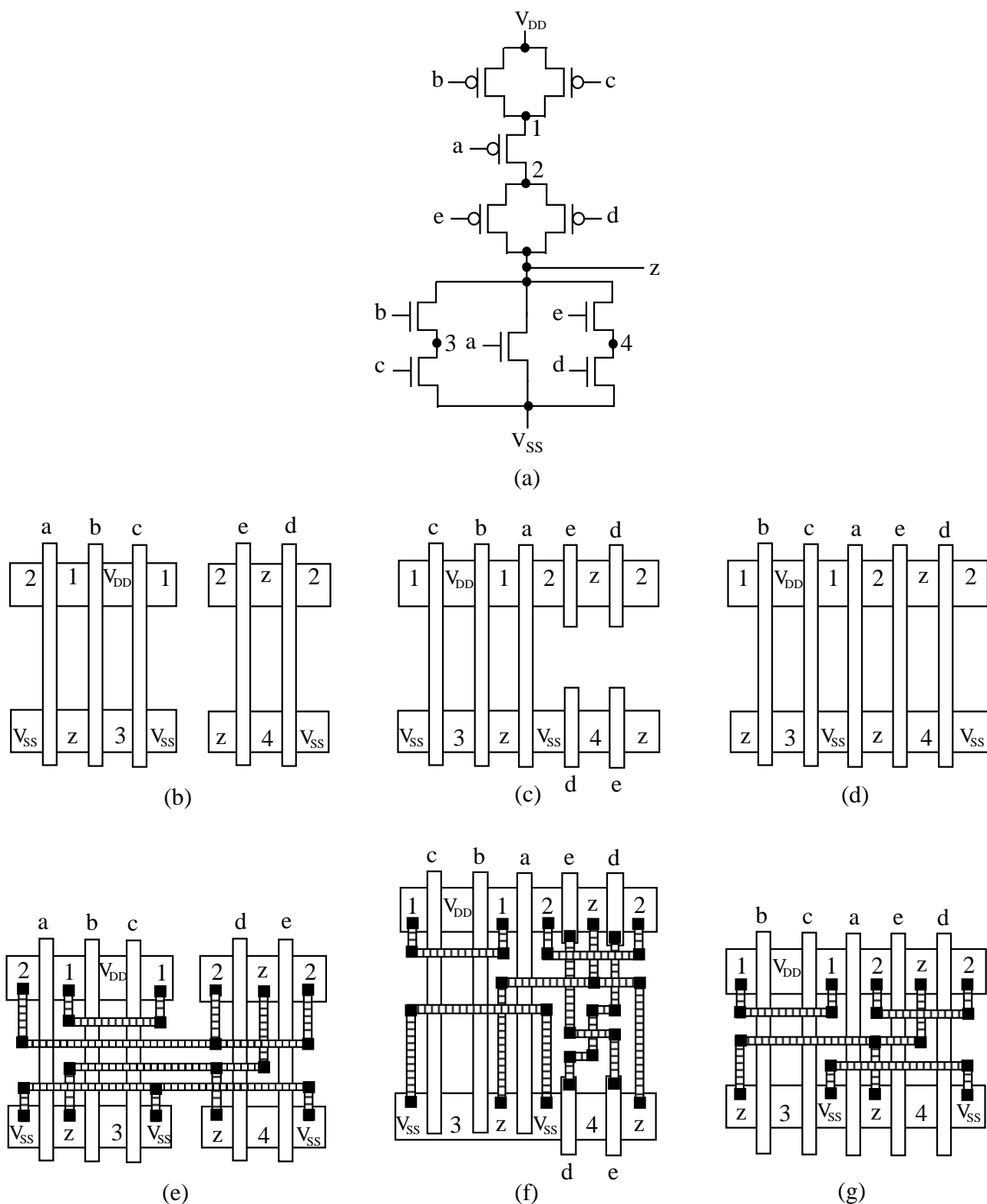


Figure 2: (a) shows a circuit implementing the function $z = a + bc + de$; (b), (c), and (d) give three alternatives of cell placement; with the respective densities of 4, 4, and 3 and the estimated areas of 24, 20, and 15 units; (e), (f), (g) give corresponding cell routings, with the total areas of 24, 25, and 15 units, respectively.

.SUBCKT	TEST		
MPA	2	a	1
MPB	1	b	VDD
MPC	1	c	VDD
MPD	Z	d	2
MPE	Z	e	2
MNA	Z	a	VSS
MNB	Z	b	3
MNC	3	c	VSS
MND	4	d	VSS
MNE	Z	e	4
.END			

4 Basic Output

For simplicity, design rule is not considered, and each component is treated as unit size and placed on a grid.

The text output of the basic requirement shall report the placement with the minimum estimated area, which consists of the following information:

- (1) **Cell placement information** that contains four lines; the first line gives the pMOS transistor (upper array) ordering (**use * for a diffusion gap**), the second line describes the sequence of the names of drain/source terminals in the upper array, the third line gives the nMOS transistor (lower array) ordering (**use * for a diffusion gap**), and the fourth line describes the sequence of the names of drain/source terminals in the lower array.

Here give two sample text outputs resulting from the circuit shown in Figure 2(a): one corresponds to the placement shown in Figure 2(b), which consists of a diffusion gap, and the other corresponds to the optimal placement shown in Figure 2(d).

Placement in Figure 2(b)						Placement in Figure 2(d)					
a	b	c	*	e	d	b	c	a	e	d	
2	1	VDD	1	2	Z 2	1	VDD	1	2	Z 2	
a	b	c	*	e	d	b	c	a	e	d	
VSS	Z	3	VSS	Z	4 VSS	Z	3	VSS	Z	4 VSS	

See Figures 2(b) and (d) for example graphical outputs.

- (2) **Density** of the placement.
- (3) **Estimated area** of the placement.

5 Advanced Features/Functions

You are free to incorporate the following advanced features/functions in your tool. Possible advanced features/functions includes:

- **Routing:** Assume the two-layer metal routing model, with one layer (metal-1) reserved for horizontal wires and the other (metal-2) for vertical ones, and complete the routing. Note that a contact via is required for connecting the same net in different layers. See Figures 2(e), (f), and (g) for three example routing configurations.

- Diffusion gap parameter:** In the basic requirement, we worked on the area model of one diffusion gap equal to one polysilicon column. In future technology, it is possible that the area of a diffusion gap is significantly larger than that of a polysilicon column. Therefore, it is desirable to employ a more sophisticated area model by specifying a positive integer weight for diffusion gaps, say α , $\alpha \in \mathbb{Z}^+$. Now width W is given by the following formula:

$$W = C + \alpha G, \tag{3}$$

where C and G are the numbers of polysilicon columns and diffusion gaps, respectively.

- Incremental update:** Layout engineers often need to perform incremental updates for a layout design. Typical operations include inserting/deleting/moving one or a set of transistors, splitting/merging/swapping a pair of transistors, etc. Each such operation may alter the dimension and area of a cell. It is thus useful to develop those features to guide an engineer to make wise decisions in layout design. Figure 3 shows several typical updates.

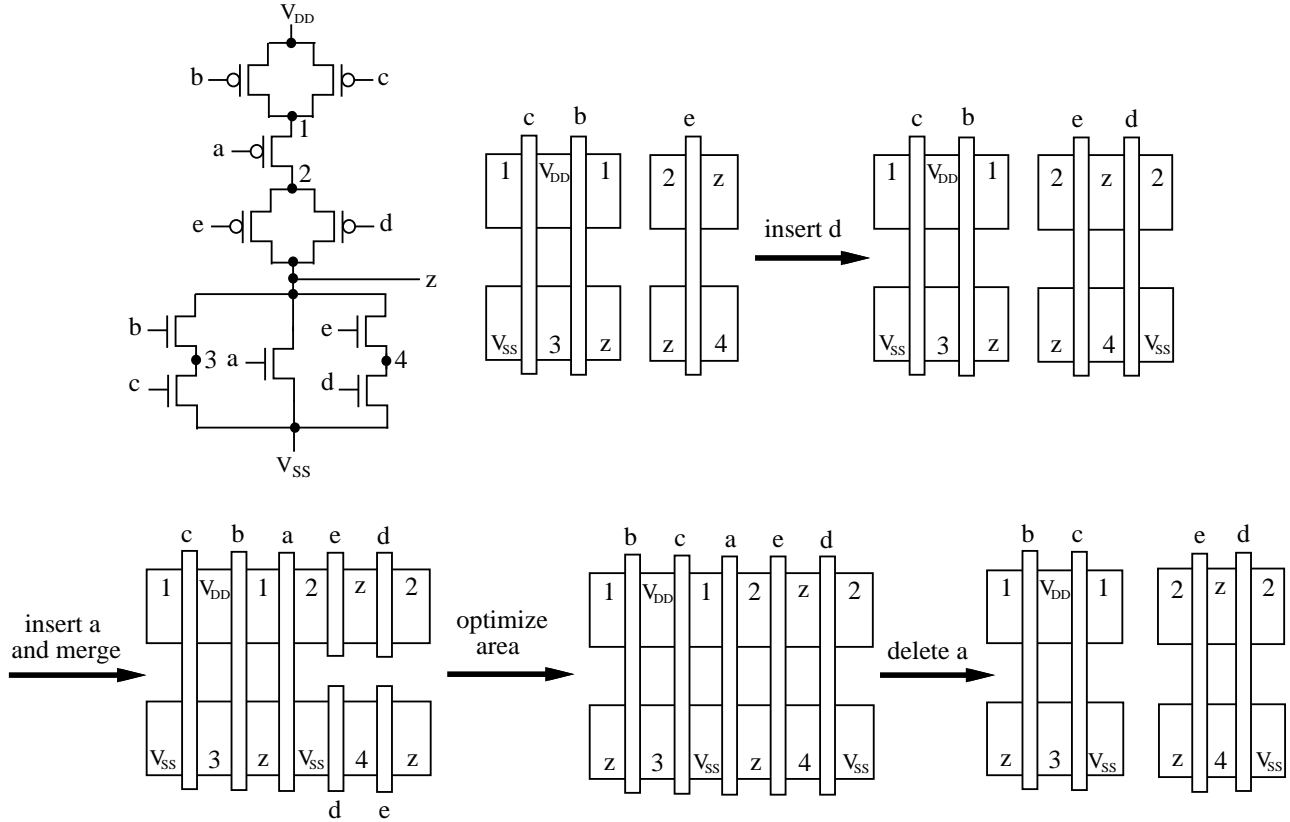


Figure 3: Incremental updates of a layout.

- User interface:** The tool may provide insertion, deletion, split, merge, move, and/or swap functions and some editing features such as undo/redo. This tool may behave as follows: Initially, it shows part or the whole design (can be placed by the tool or in a predefined order). After a user performs an operation, the tool will report the current layout information (width, the number of diffusion gaps, density, height, etc) and possible changes of other transistors to reach the minimum area. Also, a user can specify which transistors to be fixed or which transistors can be moved.

6 Language/Platform

- Language: C or C++.
- Platform: SUN OS/Solaris or PC DOS/Windows.

7 Evaluation

- Correctness, layout area, time and memory consumption, advanced features/functions, user interface, etc.

8 Questions

Please report any question regarding this problem to `cad@cis.nctu.edu.tw` with the email subject "CAD Contest: Problem 7." Your question(s) will be answered in two weeks, and the Q&A's will be posted at the contest web site.

References

- [1] Hwang, C. Y., Y. C. Hsieh, Y. L. Lin, and Y. C. Hsu, "An Optimal Transistor-Chaining Algorithm for CMOS Cell Layout," *Proc. of International Conference on Computer-Aided Design*, pp. 344–347, Nov. 1989.
- [2] R. L. Maziasz and J. P. Hayes, *Layout Minimization of CMOS Cells*, Kluwer Academic Publishers, 1992.
- [3] R. L. Maziasz and J. P. Hayes, "Layout optimization of CMOS functional cells," *Proc. 24th Design Automation Conference*, pp. 544–551, June 1987.
- [4] R. L. Maziasz and J. P. Hayes, "Layout optimization of static CMOS functional cells," *IEEE Transactions on Computer-Aided Design*, vol. CAD-9, pp. 708–719, July 1990.
- [5] R. L. Maziasz and J. P. Hayes, "Exact width and height minimization of CMOS cells," *Proc. 28th Design Automation Conference*, pp. 487–493, June 1991.