

Problem P8 : Pattern generator for Built-in self-test

Contestant : A50

Test circuits : p8_1.v, p8_2.v, p8_3.v

Output requirement :

1. Verilog netlist of PRPG.
2. output pattern of the PRPG in VCD format.

Test strategy : Given a valid VCD, we use Syntest fault simulator to fault grade the circuit.

Results :

1. Given the necessary information of the circuit, the program generates a PRPG circuit and the VCD output.
2. The contestant does not run its program on the test circuits (p8_1.v, p8_2.v, p8_3.v).
3. The program does not take into account the number of primary inputs of the circuit. It is also not explained in the report how they want to connect the PRPG and the orig circuit. In order to get the fault coverage figures, we replace the PRPG in the Syntest Logic Bist architecture with the generated PRPG. We get the following:

CIRCUIT p8_1:

This circuit has 1000 test patterns and contains 602 UNCOLLAPSED faults of which 562 (93.36%) faults were Hard detected (HD).

0 (0.00%) data faults were Potentially testable (PT).

0 (0.00%) clock/enable faults were Potentially untestable (PU).

13 (2.16%) Untestable (UT) faults were Ignored (IG) or Tied to VCC/GND.

0 (0.00%) Untestable (UT) faults were Uncontrollable.

0 (0.00%) Untestable (UT) faults were Blocked (Unobservable).

0 (0.00%) Untestable (UT) faults were due to circuit design.

27 (4.49%) faults were Undetected (UD).

fsm pessimistic fault coverage = $HD/(Total-IG)$ = 95.4160 %.
 fsm pessimistic test coverage = $HD/(Total-UT)$ = 95.4160 %.
 fsm pessimistic test efficiency = $(HD+UT)/Total$ = 95.5150 %.

 fsm optimistic fault coverage = $(HD+PT)/(Total-IG)$ = 95.4160 %.
 fsm optimistic test coverage = $(HD+PT)/(Total-UT-PU)$ = 95.4160 %.
 fsm optimistic test efficiency = $(Total-UD)/Total$ = 95.5150 %.

CIRCUIT p8_2:

This circuit has 5000 test patterns and contains 255810 UNCOLLAPSED faults of which 203061 (79.38%) faults were Hard detected (HD).

0 (0.00%) data faults were Potentially testable (PT).

0 (0.00%) clock/enable faults were Potentially untestable (PU).

6572 (2.57%) Untestable (UT) faults were Ignored (IG) or Tied to VCC/GND.

0 (0.00%) Untestable (UT) faults were Uncontrollable.

3340 (1.31%) Untestable (UT) faults were Blocked (Unobservable).

461 (0.18%) Untestable (UT) faults were due to circuit design.

42376 (16.57%) faults were Undetected (UD).

fsm pessimistic fault coverage = $HD/(Total-IG)$ = 81.4727 %.
 fsm pessimistic test coverage = $HD/(Total-UT)$ = 82.7345 %.
 fsm pessimistic test efficiency = $(HD+UT)/Total$ = 83.4346 %.

fsm optimistic fault coverage = $(HD+PT)/(Total-IG)$ = 81.4727 %.
 fsm optimistic test coverage = $(HD+PT)/(Total-UT-PU)$ = 82.7345 %.
 fsm optimistic test efficiency = $(Total-UD)/Total$ = 83.4346 %.

CIRCUIT p8_3:

This circuit has 2000 test patterns and contains 176656 UNCOLLAPSED faults of which 150140 (84.99%) faults were Hard detected (HD).

1456 (0.82%) data faults were Potentially testable (PT).

1180 (0.67%) clock/enable faults were Potentially untestable (PU).

4211 (2.38%) Untestable (UT) faults were Ignored (IG) or Tied to VCC/GND

2876 (1.63%) Untestable (UT) faults were Uncontrollable.

11547 (6.54%) Untestable (UT) faults were Blocked (Unobservable).

7 (0.00%) Untestable (UT) faults were due to circuit design.

5239 (2.97%) faults were Undetected (UD).

fsim pessimistic fault coverage = $HD/(Total-IG)$ = 87.0654 %.

fsim pessimistic test coverage = $HD/(Total-UT)$ = 95.0163 %.

fsim pessimistic test efficiency = $(HD+UT)/Total$ = 95.5422 %.

fsim optimistic fault coverage = $(HD+PT)/(Total-IG)$ = 87.9098 %.

fsim optimistic test coverage = $(HD+PT)/(Total-UT-PU)$ = 96.6595 %.

fsim optimistic test efficiency = $(Total-UD)/Total$ = 97.0343 %.

Note: The result is not bad.

Problem P8 : Pattern generator for Built-in self-test

Contestant : A57

Test circuits : p8_1.v, p8_2.v, p8_3.v

Output requirement :

1. Verilog netlist of PRPG.
2. output pattern of the PRPG in VCD format.

Test strategy : Given a valid VCD, we use Syntest fault simulator to fault grade the circuit.

Results :

1. The input format to the program is unknown to us (.st). It is not explained anywhere in the report how this input format can be generated. We can not do anything with it.

Note: I just got an e-mail from the student saying that they do not complete the conversion program.

2. The contestant does not run its program on the test circuits (p8_1.v, p8_2.v, p8_3.v).
3. It seems like they are implementing the work described in the paper "Altering a pseudo-random bit sequence for scan-based BIST", by Toubia, N.A and McCluskey, E.J in Proceedings of ITC'96.

Although the work is not original, the package itself is still quite impressive. Unfortunately does not read in the test circuits nor generate the required outputs.