IC/CAD Contest

Problem 2: Two-way Mincut Partitioning Problem

Source: Avant!, Taiwan

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1 Introduction

Let $C = \{C_1, C_2, ..., C_n\}$ be a set of cells and $N = \{N_1, N_2, ..., N_m\}$ be a set of nets. Each net N_i, $i = 1, 2, ..., m$, connects a subset of the cell set. The two-way mincut partitioning problem is to partition the cell set into two groups A and B. The size of group A, $size(A)$, is the number of cells in group A. $Size(B)$ is the number of cells in group B. Partition is also referred to as a cut. The cost of partition is called cut-size, which is the number of nets across the cut, i.e. having cells in both groups. The goal is to minimize the cut-size. The constraint is that the difference between $size(A)$ and $size(B)$ must be smaller than one percent of the total number of the cells in the cell set.

2 Problem Description

Two-way Mincut Partitioning Problem is defined as follows.

- **Input:** A net-list for a circuit
- **Objective:** To partition the circuit to two subcircuits A and B so that the cut-set of subcircuits A and B is minimized under the constraint of $|size(A) - size(B)| < \frac{1}{100} \cdot n$, where n is the number of cells in the circuit.

3 Input

Input is a list of nets. Each net statement starts with the keyword "NET" and the name of the net. The cells that are connected by the net are listed between a pair of braces following the net name.

Example:
NET n1 c2 c3 c4
NET n2 c3 c7
NET n3 c3 c5 c7
NET n4 c1 c3 c5 c7
NET n5 c2 c4 c8
NET n6 c4 c6
NET n7 c2 c6 c8

4 Output

Report the cells in each group and the cut-size. The format is free.

Example:
Group A = c1 c3 c5 c7
Group B = c2 c4 c6 c8
Cut-size = 1

5 Language/Platform

- Language: no restriction.
- Platform: SUN workstation (Sparc) is preferred.

6 Evaluation

- Reported cut-size: 50%
- CPU time and memory usage: 50% (Please expect that the problem size could reach 500K cells.)

7 Questions

Please report any questions regarding this problem to `cad@cis.nctu.edu.tw` with the email subject "CAD Contest: Problem 2." Your question(s) will be answered in two weeks, and the Q&A's will be posted at the contest web site

References

[1] Naveed Sherwani, *Algorithms for VLSI Physical Design Automation* , Second Edition, Kluwer Academic Publishers, 1996

[2] C.M. Fiduccia and R.M. Mattheyses, "A Linear-Time Heuristic for Improving Network Partitions," *19th Design Automation Conference*, 1982