

Problem 6: Static Timing Verification

Source: Faraday Technology

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1 Introduction

The purpose of this problem is to build a Static Timing Analysis (STA) Tool for synchronous sequential circuits. The STA provides “accurate” timing information for all timing paths in the circuit by tracing critical paths, and calculating maximum arrival times to points of interests. It also uses the values in the critical paths to evaluate the design constraints and create a timing report which finds violations of design constraint. The inputs to the problem contain a verilog file and a constraint file. The verilog file describes an interconnection of library cells whose delays are given. The constraint file describes the clock period and require time for all outputs, from which one can calculate the slack values for each output.

To simplify the formulation of this problem, a library (in the following) with a set of library cells and the corresponding delays are given. The delay model is assumed to be constant, i.e., the delay of a path is equal to summation delays of all cells in the path. All other delays such as the connection delay and the transition delay are neglected. Also, false paths (under floating mode model) should also be identified and excluded in the calculation of circuit delay.

CAD_CONTEST_LIB

Cell_name	Cell_function	Cell_delay
INV1	!a	1
INV2	!a	2
NAND2	!(ab)	2
NAND3	!(abc)	3
NOR2	!(a+b)	2
NOR3	!(a+b+c)	3
DFF	D flip-flop	setup time and hold time are both 1 and clk to Q delay is 1.

2 Input

The final results of this problem are to be compared with the results of DesignTime (Synopsys.) All input and output formats are similar to those in Synopsys.

- Gate level net-list. (A verilog file)
- Constraint file. (A script file)

Example:

- Gate level net-list.

```
...
input input0, input1;
output output0;
```

```

wire net1, net2;

INV1 U1(.a(input0), .z(net1));
NAND2 U2(.a(input1), .b(net1), .z(net2));
NOR2 U3(.a(net1), .b(net2), .z(output0));
...

```

- Constraint file.
set_max_delay 0 -to all_outputs();
Create_clock -period 10 -name clk1;

3 Output

Similar to the report_timing in DesignTime. Setup/Hold time violation report for each net on the critical path. (DesignTime output format)

Example:

Startpoint:
Endpoint:
Path Group: CK01

Point	Fanout	Incr	Path
...
Z (net)	6		
ABC/I(BUF)		0.21	1.74
ABC/O(BUF)		0.78	2.52
...
data required time			81.75
...
data arrival time			-15.45
slack			66.30

4 Language/Platform

- Language: no restriction.
- Platform: SUN workstation (Sparc) is preferred.

5 Evaluation

The results are to be compared with the Design Time. The more similar to the Design time, the higher score is given. False path identification is a plus.

6 Questions

Please report any questions regarding this problem to cad@cis.nctu.edu.tw with the email subject "CAD Contest: Problem 6." Your question(s) will be answered in two weeks, and the Q&A's will be posted at the contest web site

References

- [1] Srinivas Devadas, Abhijit Ghosh, Kurt Keutzer, *Logic Synthesis*, McGraw-Hill Series on Computer Engineering, 1994.
- [2] De Micheli, *Synthesis and Optimization of Digital Circuits*, McGraw-Hill Series on Computer Engineering, 1994.
- [3] Design Compiler Reference Menu.
- [4] H.C, Chen, D.Du, "Path Sensitization in Critical Path Problem," *IEEE Trans. Computer-Aided Design*, VOL 12, No. 2, pp. 196-207, 1993.